SEMICONDUCTOR MEMORY PIPELINE BUFFER

ABSTRACT

A high capacity, fast access dynamic random access memory is provided. Furthermore, a pipelined write method can be realized at each array block by affixing a latch between the sense amplifier and write data line for each column. In this manner, a data write phase can occur simultaneously with the pre-read phase of the following address. Using this method, the effective access speed to the array block can be increased, yielding a fast access cache memory.